A High Efficiency 0.25-μm CMOS PA with LTCC Multi-layer High-Q Integrated Passives for 2.4 GHz ISM Band

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***Abstract* — We present the first high efficiency CMOS power amplifier utilizing fully integrated multi-layer Low Temperature Co-fired Ceramic (LTCC) high-Q passives for 2.4 GHz ISM band applications. The inductor and capacitor library was built in a multi-layer LTCC board using a compact topology. An inductor Q-factor as high as 110 with a self-resonant-frequency (SRF) as high as 12 GHz was demonstrated. Measured results of the CMOS-LTCC PA show 45 % power added efficiency, 23 dBm output power and 18 dB gain at 2.4 GHz with a low 2.5 V drain supply voltage. This result is the first significant step toward a compact transceiver module development utilizing fully integrated multi-layer LTCC high-Q passives and a deep sub-micron (0.25 μm) CMOS technology.**

I. INTRODUCTION

During the past decade, the requirement for high-level circuit integration and high frequency operation has motivated prominent advancements in commercial silicon CMOS technologies [1]-[2]. The cost effectiveness and performance improvement of a standard deep sub-micron CMOS process make it highly attractive for mobile applications such as Bluetooth, Home RF, WDCT (Worldwide Digital Cordless Telecommunications), and upband DECT in 2.4 GHz ISM band wireless communications. Most of the efforts in commercial CMOS RF transceiver module development in this frequency band focus on size reduction and full integration. Recently, a two-chip transceiver solution for 2.4 GHz wireless communication applications has been presented based on a conventional CMOS technology [3]. This chip needs to be integrated with off-chip filters, balun and discrete passive elements, such as chip inductors and capacitors, to build a complete RF transceiver module. In addition to the integration with off-chip passive components, it requires integration with a medium power amplifier for use in the outdoor environment requiring up to 20 dBm output power.

A major hindrance for full integration onto a single chip using standard CMOS technologies is the fact that the on-chip passives, such as inductors, capacitors, and filters, require high-Q values. Multi-layer LTCC is one of the compact and cost-effective solutions to this problem. It is attractive to implement a complete RF transceiver module for 2.4 GHz ISM band based on a standard deep sub-micron CMOS technology with LTCC passives in order to replace low-Q passives on silicon [4] with multi-layer high-Q passives such as inductors [5], filters [6]-[7] and antenna [8]. The availability of high-Q passives demonstrates that the LTCC is a good candidate for system-on-package (SOP) solutions [9].

This work presents the design and testing of a high efficiency 2.4-GHz CMOS-LTCC power amplifier. The technology employed is based on a low loss LTCC and a standard deep sub-micron (0.25 μm) CMOS process. We show the measured result of the first reported high efficiency 2.4 GHz CMOS PA utilizing fully integrated multi-layer LTCC passives. This PA can easily be used in a complete 2.4 GHz RF transceiver module that requires medium power output for outdoor wireless communication systems utilizing constant envelope modulation schemes. For implementing this power amplifier, a custom non-linear deep sub-micron MOSFET model [10] has also been developed and incorporated into a harmonic balance simulator.

II. LTCC HIGH-Q INTEGRAL PASSIVES

We developed the LTCC inductor and capacitor library that allows high-Q passives and a higher level of integration in addition to eliminating the assembly time and cost incurred by the discrete off-chip components. LTCC-based lumped-element component library has been described in [11]. The inductor components were designed based on a multi-layer ground plane concept where the microstrip inductor footprints were printed on the surface layer. Multiple inductance values can be obtained by moving the location of the ground plane, thereby tailoring the shunt parasitic capacitance to ground to achieve different effective inductance using the same lateral area of inductor footprints. However, the discontinuous nature of the ground plane located in different layers causes

additional parasitic mechanisms that are not easily modeled in simulation.

In this paper, we fix the location of the ground plane on the backside metal of the board, thereby establishing a continuous ground plane for the entire circuit. Since the ground plane layer is fixed, in order to realize multiple inductance values with the same lateral area, in some cases the inductor footprints need to be buried. This topology is established in a twenty-layer LTCC tapes utilizing the recently introduced Dupont 943AT technology. Each tape has a thickness of 4.4 mils with 7 μm gold and silver paste metallization. Fig. 1 shows a quality factor and effective inductance of one of the inductors fabricated in the LTCC board. The Q and SRF are around 110 and 12 GHz with a corresponding effective inductance of 1.1 nH at 2.4GHz.

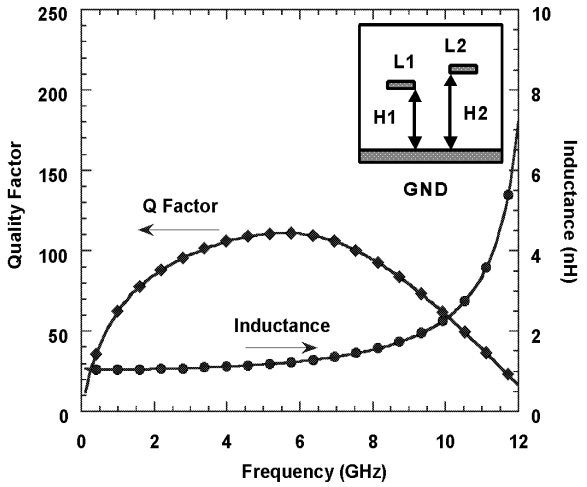

Fig. 1. Quality factor and effective inductance of the fabricated LTCC inductor. Inset shows the inductor structure. Two different inductors (L1 and L2) can be obtained by varying the distance (H1 and H2) between each inductor metal to the ground.

For the capacitors, both Metal-Insulator-Metal (MIM) and Vertically Interdigitated Capacitor (VIC) [11] have been incorporated into the design. This VIC structure implements a capacitor by stacking and intertwining electrodes in a multi-level dielectric system. Such a configuration is suitable for realizing a large capacitance, such as the RF ground capacitor, in a multi-layer board. Stacking and intertwining multiple electrodes is equivalent to establishing parallel capacitor interconnects whose total capacitance is the sum of the individual capacitances formed by pairs of electrodes.

The VIC topology has been shown to save considerable real estate especially when used to implement large capacitors such as the RF ground capacitors. Since VIC topology requires additional interconnects for the intertwined capacitor electrodes deployed on different layers, additional loss and parasitic inductance are expected. These facts degrade the Q and SRF performance. Therefore, in our design, VICs were only used to implement RF ground at 2.4 GHz while MIM capacitors were used in matching networks. Fig. 2 shows the Q and effective capacitance of the LTCC capacitors used in the PA design demonstrating Q and SRF of 150 (at 2.4 GHz) and 7 GHz. The LTCC passives were designed using a commercial electromagnetic simulator [12] and represented as an equivalent circuit model in a harmonic balance simulator.

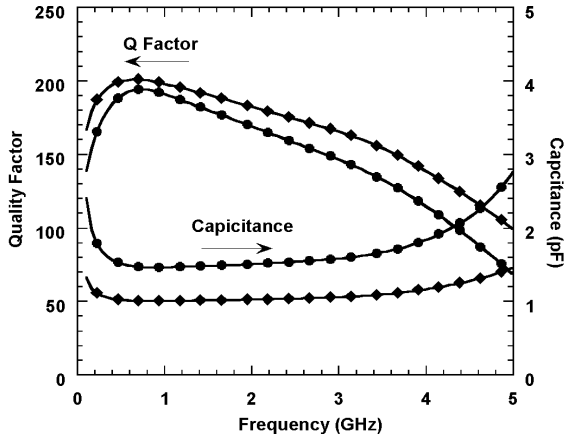

Fig. 2. Quality factor and effective capacitance of the fabricated LTCC capacitors: 1.1 pF (◆) and 1.9 pF (●).

In addition to the passive library, a custom RF/microwave non-linear MOSFET model [10] for large signal applications has also been developed for power amplifier design, which is compatible with standard commercial wireless CAD tools. This improved RF nonlinear model incorporates the breakdown voltage turnover behavior into a continuously differentiable channel current model, and a new nonlinear coupling network between the drain and lossy substrate. The complete large signal model was implemented in a harmonic balance simulator and incorporated in the high efficiency CMOS-LTCC power amplifier simulation.

III. CMOS-LTCC Power Amplifier Design

A two-stage 2.4 GHz power amplifier with second-harmonic tuning circuits on the output of each stage using silicon deep sub-micron N-MOSFETs has been developed using the low loss LTCC passive library. Fig. 3 shows the circuit schematic of the LTCC power amplifier, which is designed to operate from a single 2.5 V supply.

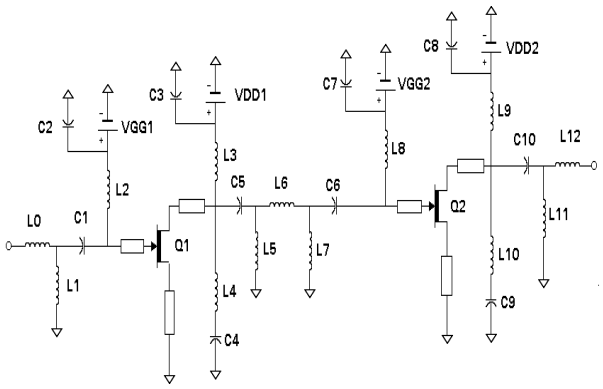

Fig. 3. 2.4 GHz high efficiency CMOS-LTCC PA circuit diagram.

The design is performed based on the dynamic load-line graphical method using nonlinear simulator, utilizing nonlinear device model and LTCC passive model to optimize the power amplifier performance. A single-ended two-stage common source amplifier is implemented with an LTCC integrated reactive matching network using multi-layer LTCC high-Q passives. For the high efficiency operation, a low DC biasing is required. Each stage of the PA was biased in class AB incorporating second-harmonic tuning circuits in the output of each stage.

Fig. 4 shows the photograph of the CMOS-LTCC power amplifier. The two deep sub-micron N-MOSFET devices fabricated in a conventional 0.25-μm deep sub-micron CMOS technology [10] were wirebonded onto gold pads on the LTCC board, which is connected to the bottom ground metal through multiple via interconnections.

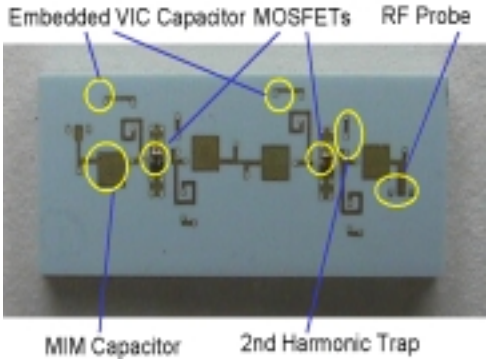

Fig. 4. Photograph of the fabricated CMOS-LTCC PA.

Using multiple bond wires from the chip to the RF ground pad minimizes the effect of bond-wire inductance, which degrades the gain and efficiency. The gate width of the first and second stage device is 1.5 mm (30 fingers) and 3 mm (60 fingers) respectively. The substrate, source and ground node are tied together eliminating body bias effects. The chip size of this power amplifier is 8 mm x 15 mm. To ensure that the driver stage does not enter power saturation region before the output stage, a slightly oversized transistor has been chosen for the first stage device. Parallel plate MIM capacitors were utilized as matching components for the fundamental signal since their values and sizes are relatively small. The RF ground capacitors were implemented in the compact VIC topology since they require large capacitance value for 2.4 GHz applications. Second-harmonic tuning elements were implemented through a series LC resonator at 4.8 GHz as part of the second-harmonic trap network to improve the power added efficiency [13].

IV. MEASUREMENT RESULTS

Fig. 5 shows the measured gain, PAE and output power of the fabricated CMOS-LTCC PA at 2.4 GHz designed by using the LTCC passive library and the custom-developed deep sub-micron MOSFET nonlinear model [10].

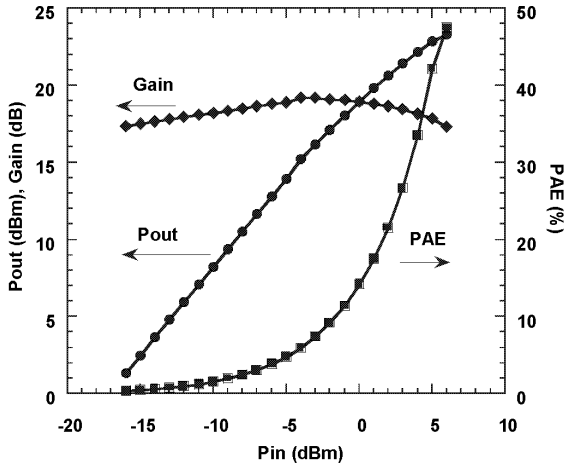

Fig. 5. Measured output power(●), gain(◆)and efficiency(■) of the fabricated CMOS-LTCC PA sweeping Pin at Vds = 2.5 V and 2.4 GHz.

The power amplifier exhibits 45 % power added efficiency, 23 dBm output power and 18 dB power gain at 2.4 GHz with a low 2.5 V drain supply voltage as indicated in Fig. 5. The 24 dBm output power is obtained at 3 dB output power compression point, at which the maximum power added efficiency is about 51 % The measured second and third harmonics are larger than 35 dBc at 1 dB compression point (P1dB) due to the second-harmonic traps and the low pass filter topology of the output matching circuit for the second stage. The measured

small signal performance of the power amplifier, showing a good return loss and a forward transfer gain, is plotted in Fig. 6.

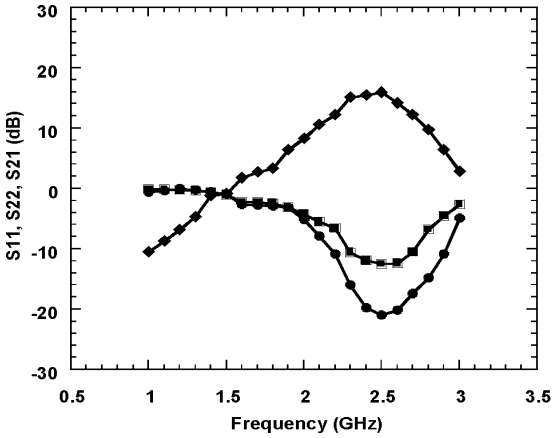

Fig. 6. Measured S11(●), s21(◆), S22(■) of the fabricated CMOS-LTCC PA at Vds=2.5 V.

Table I provides a detailed summary of the measured power amplifier performance. This CMOS-LTCC module with multi-layer integral passives is applicable to other RF transceiver modules for 2.4 GHz wireless communication applications with constant envelope modulation schemes.

TABLE I
PERFORMANCE SUMMARY OF THE MEASURED CMOS-LTCC POWER AMPLIFIER

Freqency Range	2.4 GHz to 2.5 GHz
Supply Voltage	2.5 V
Maximum Pout	23 dBm
Input VSWR	<1.5:1
Gain Variation In Band	<0.5 dB
Power Added Efficiency	45 %
Power Gain	18 dB
Harmonics	>35 dBc

V. CONCLUSION

We report the first demonstration of a high efficiency 2.4 GHz CMOS power amplifier with fully integrated high-Q LTCC passives. Under a low drain supply of 2.5 V, a PAE of 45 %, an output power of 23 dBm, and an associated gain of 18 dB were obtained at 2.4 GHz. This is a significant step toward a higher level of integration for complete, compact and cost-effective 2.4 GHz ISM band RF transceiver module development based on a standard deep sub-micron (0.25 μm) CMOS technology and fully integrated high-Q multi-layer low loss LTCC passives.

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